



Finding the Right Way for High-Performance NFV

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Agenda

1

Backgrounds

2

D-Plane Technologies

3

Performance

4

Research Directions

Virtualizing Everything

Client
Computers

1st-gen
virtualization
(Before NFV)

Edge
Functions

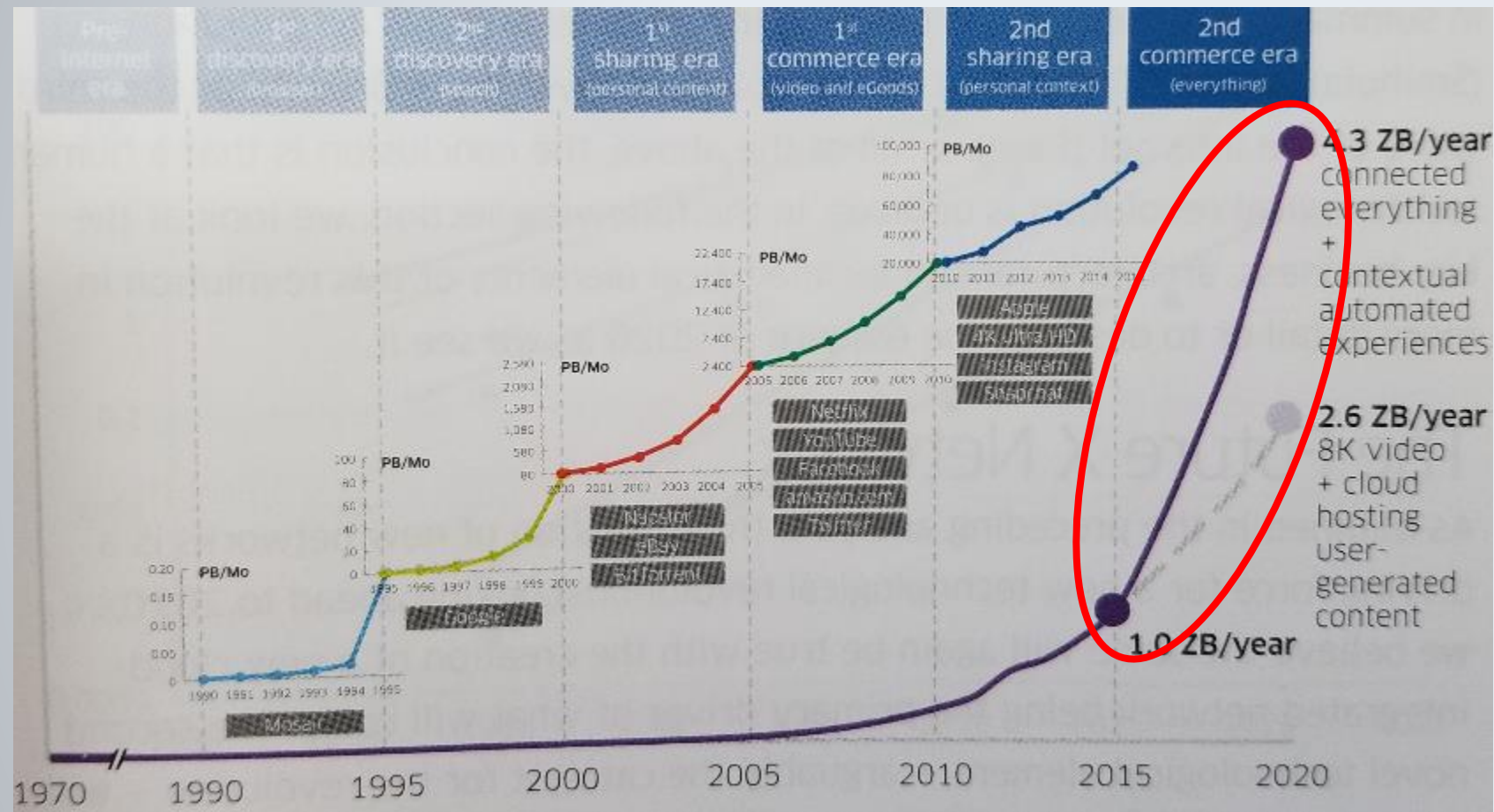
2nd-gen
virtualization
(Early-stage NFV)

Core
Functions

3rd-gen
virtualization
(Future NFV)



Core Network Traffic



Marcus K. Weldon, The Future X Network

Hardware

400G Ethernet
(IEEE 802.3bs)

Software

Next-gen. VNF?

Agenda

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D-Plane Technologies

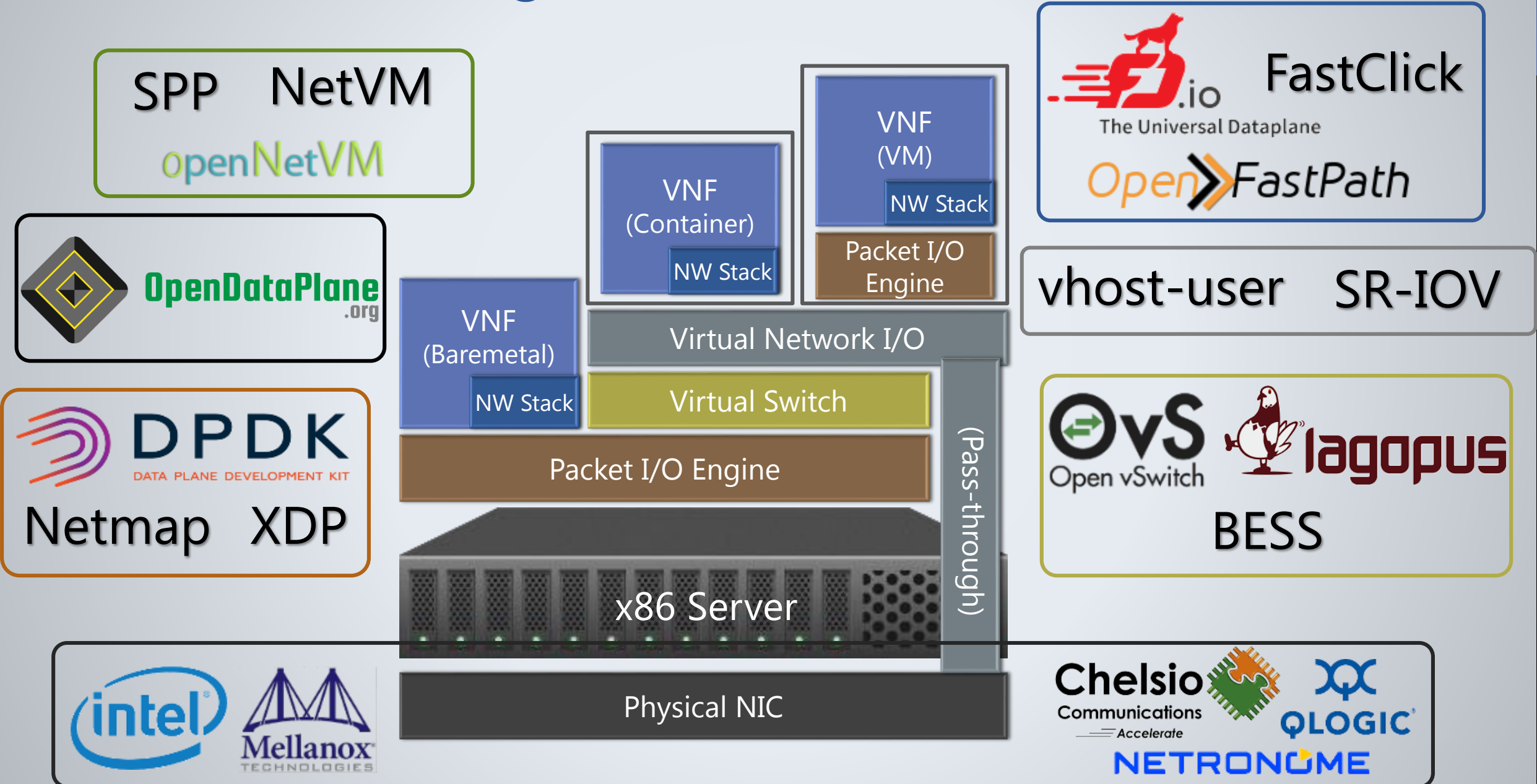
3

Performance

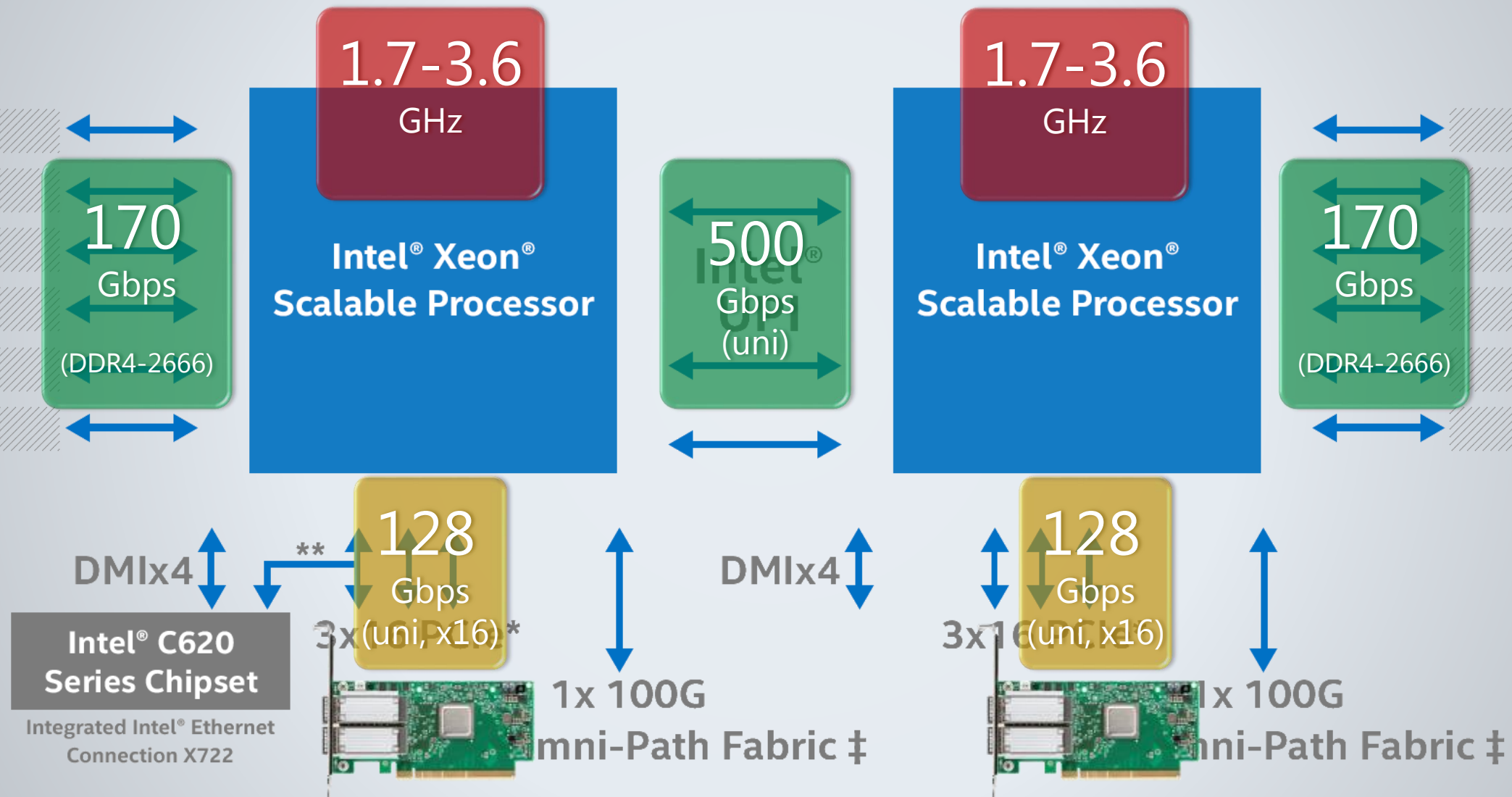
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Research Directions

D-Plane Technologies in NFV-nodes



x86 Server Architecture (Intel Xeon Scalable Processor)



Fast Packet I/O Engine



Pure Polling

Pre-allocated Memory

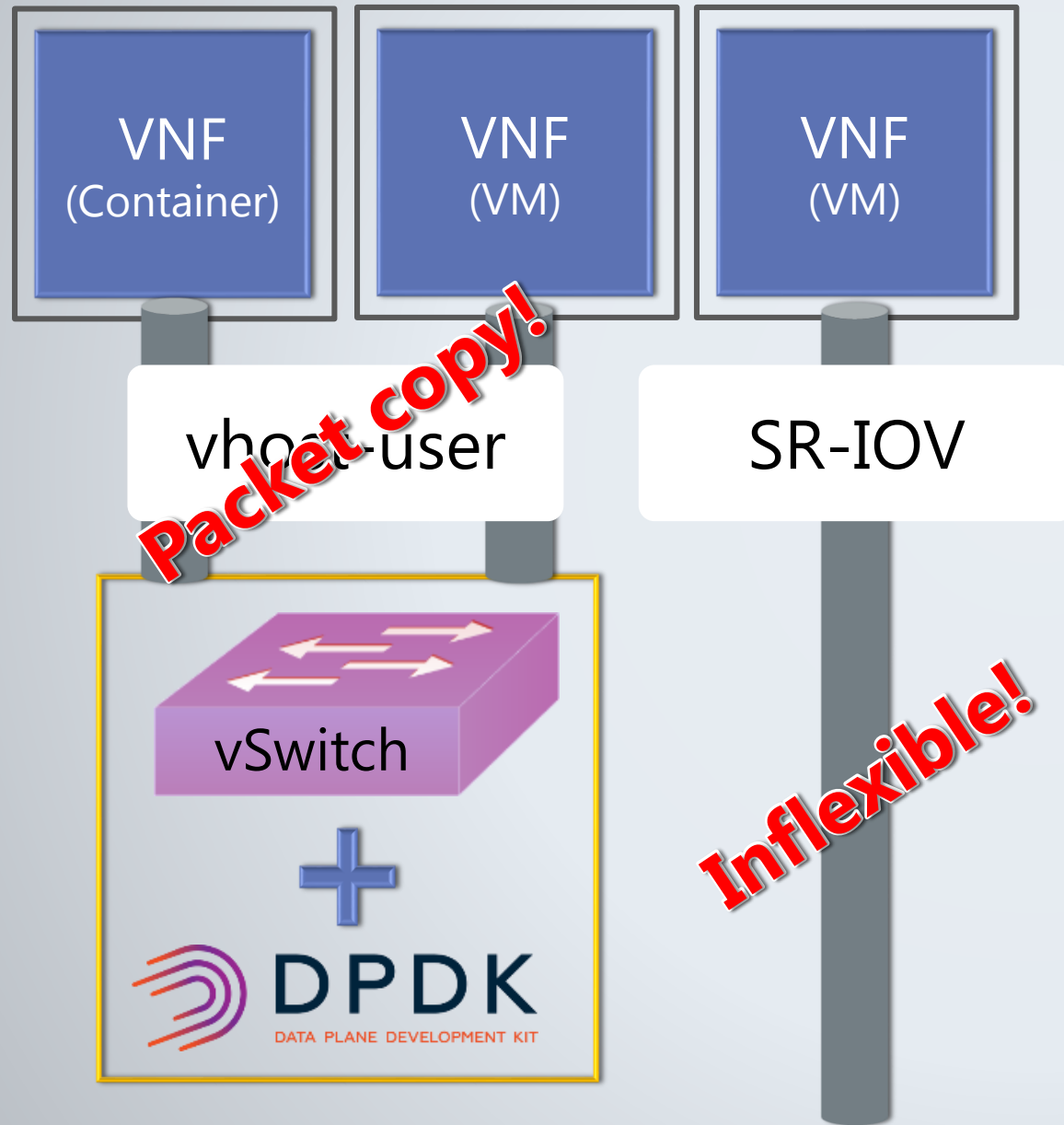
User-space DMA

Packet Batching

100% CPU usage!



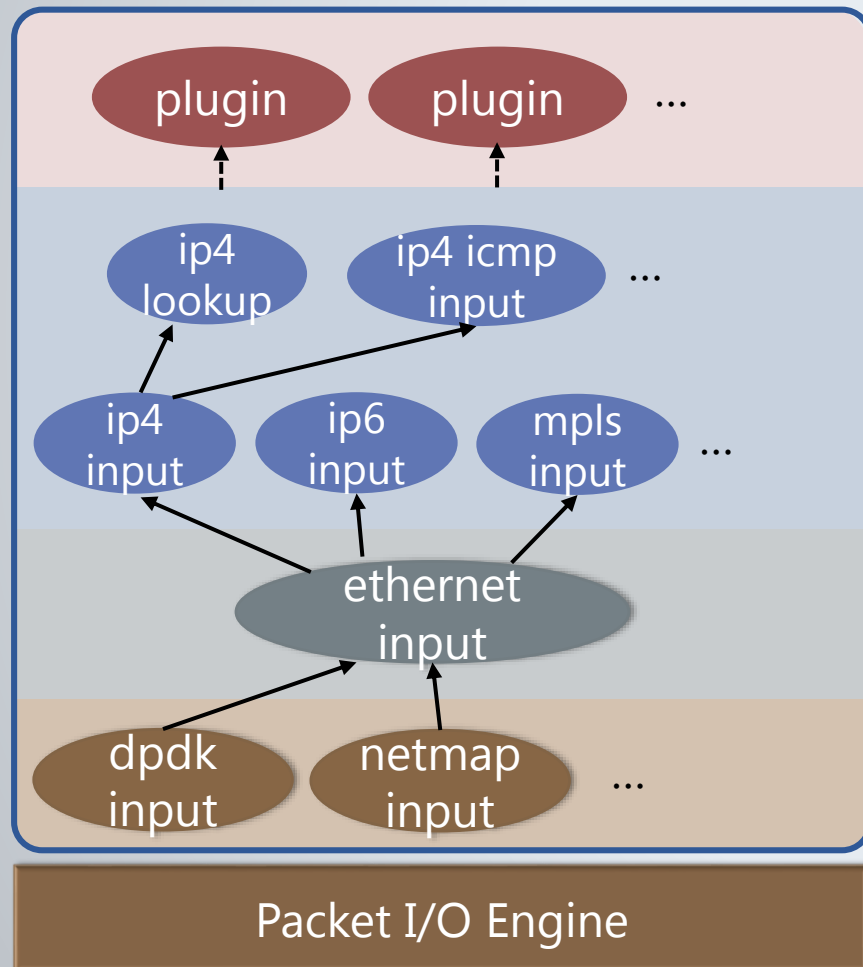
Bridging VNFs and the Host



Inflexible!

User-space Network Stack

Vector Packet Processing (VPP)

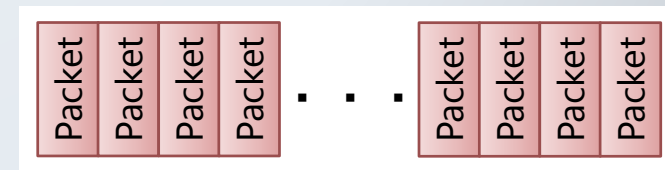


Full network stack

Click-like modular design

Vectorized processing

Packet Vector



(N: 4 - 256)

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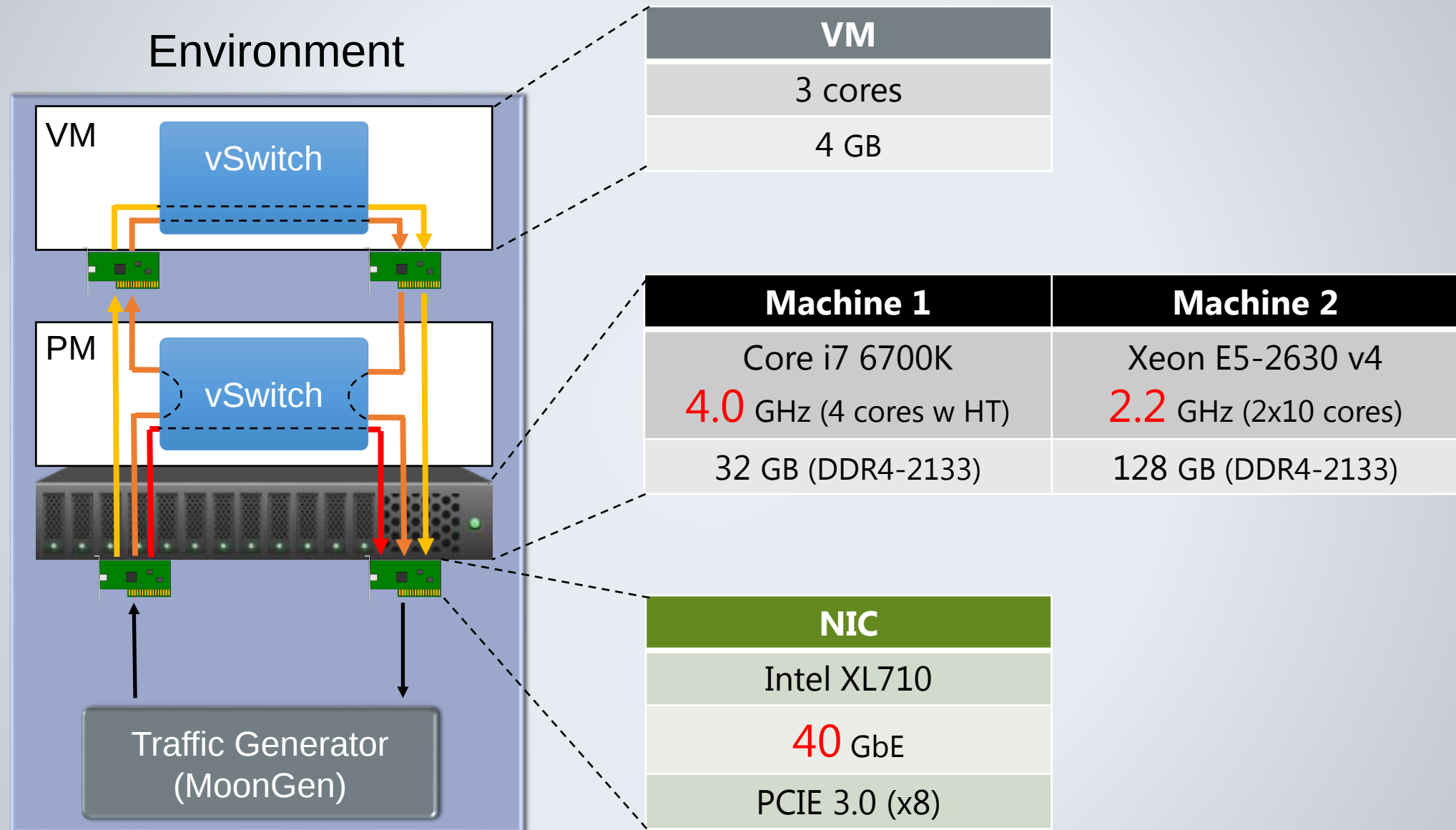
3

Performance

4

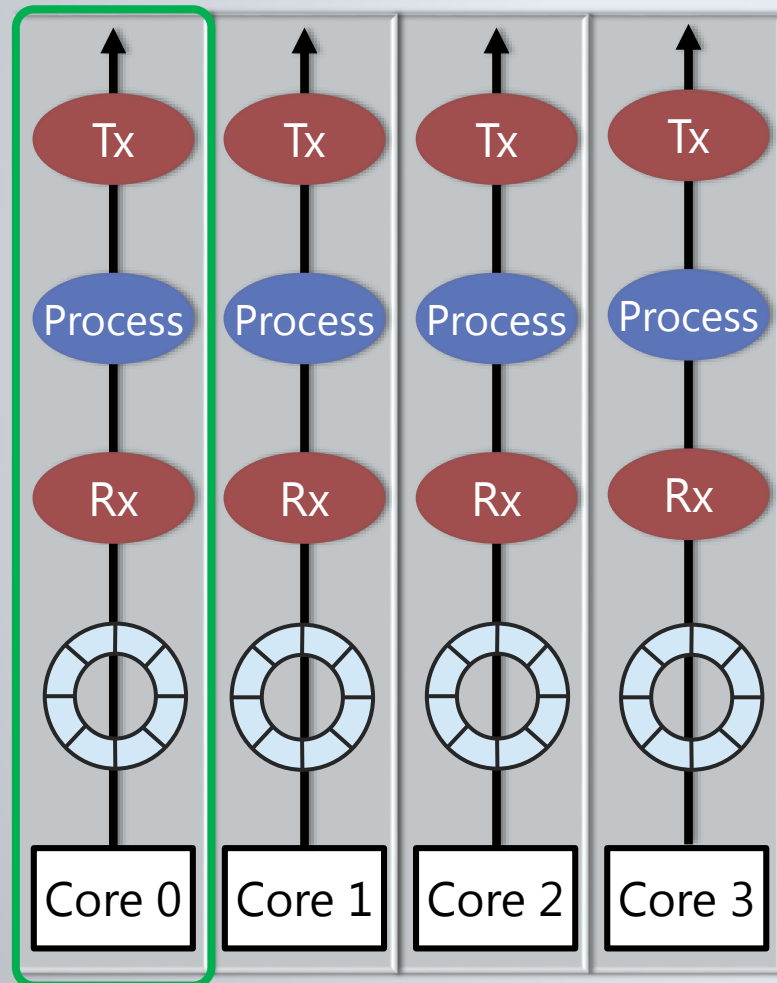
Research Directions

Evaluation



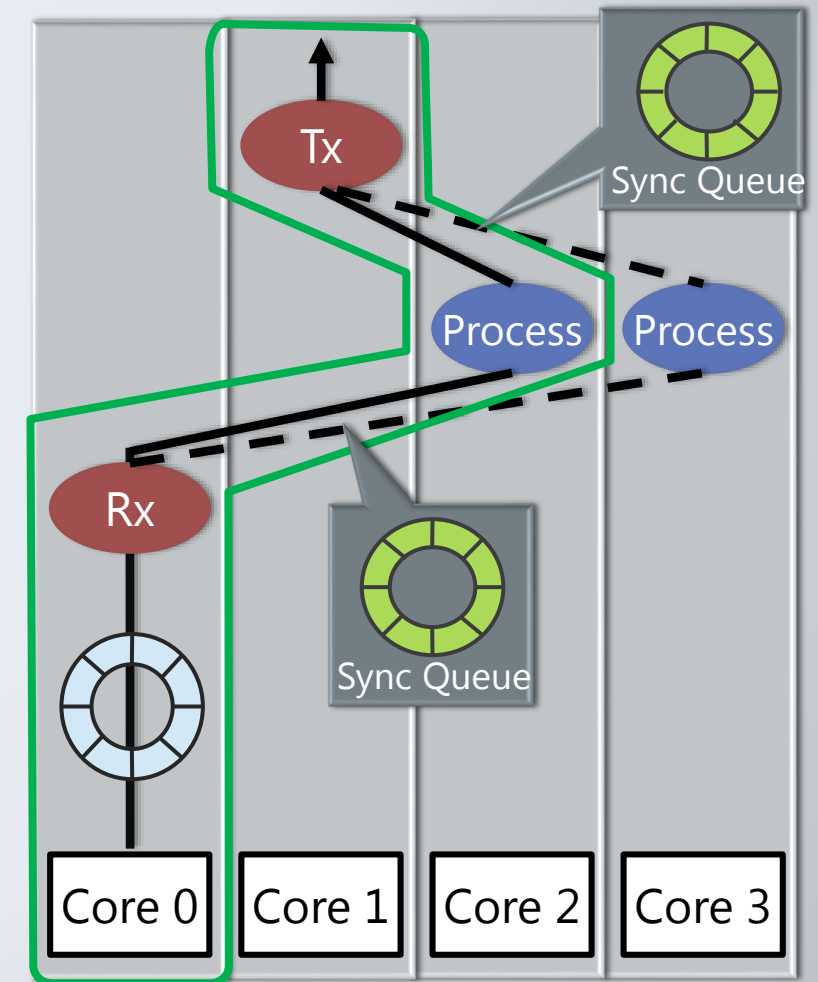
LFMT (Lock-free Multi-threading)

Run-to-Completion



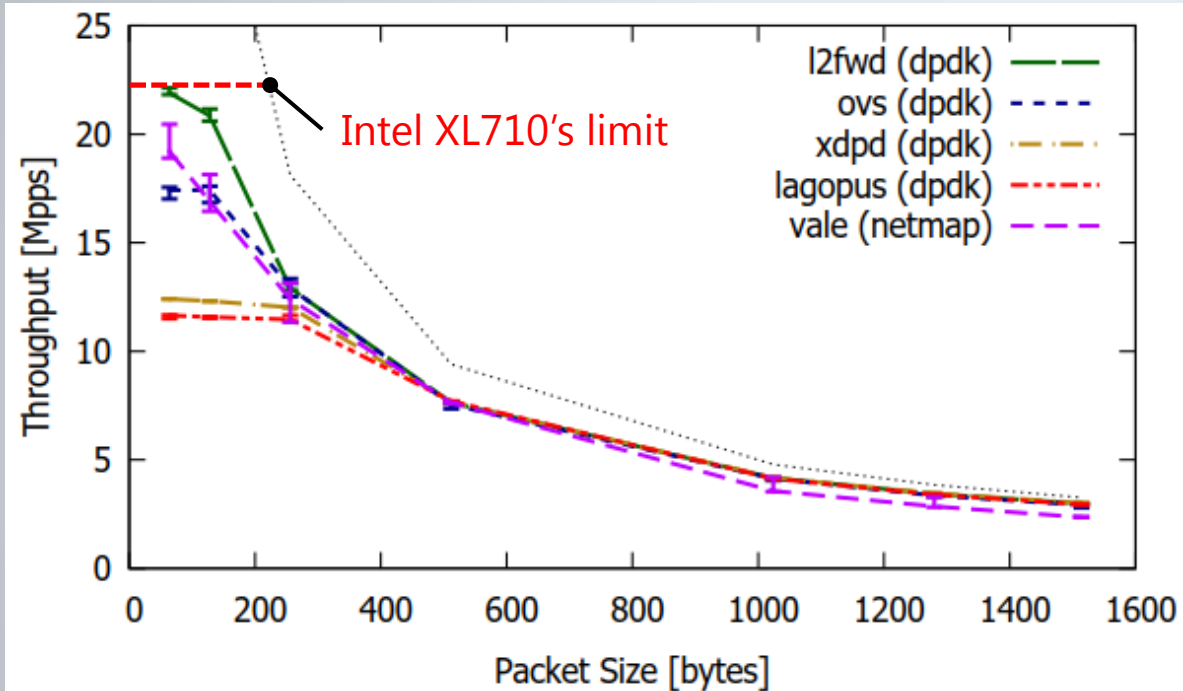
Lock free!
Scale out!

Pipeline

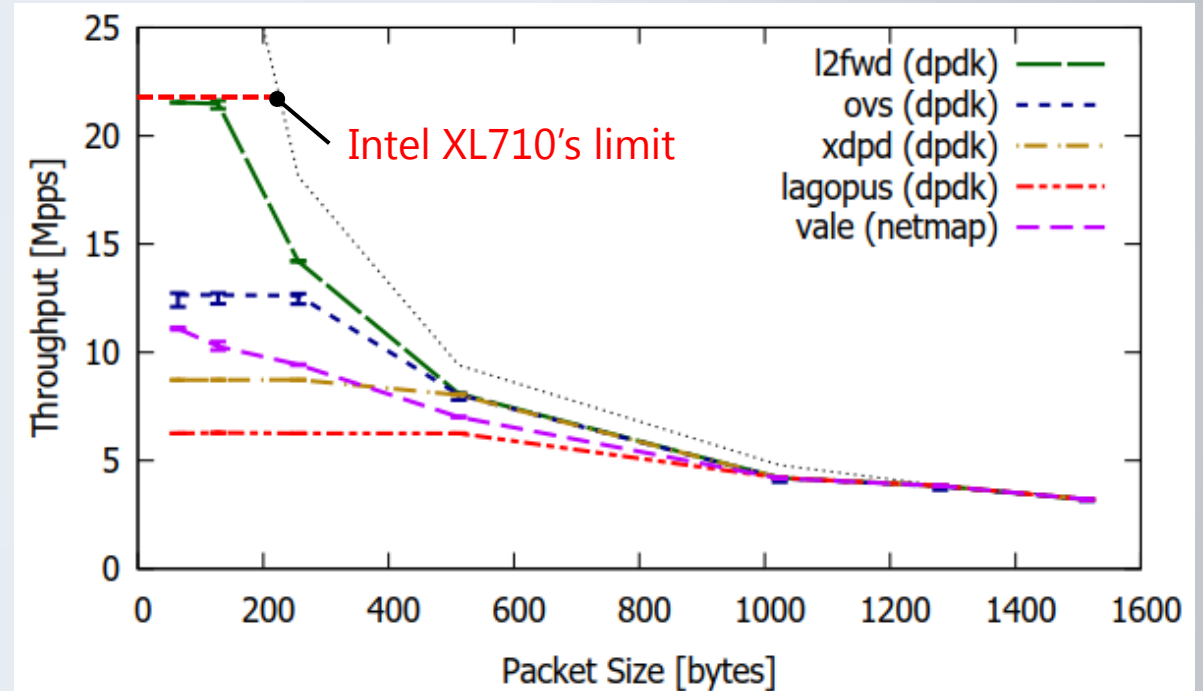


Phy-to-Phy Throughput (Baremetal)

Machine 1 (4.0 GHz)



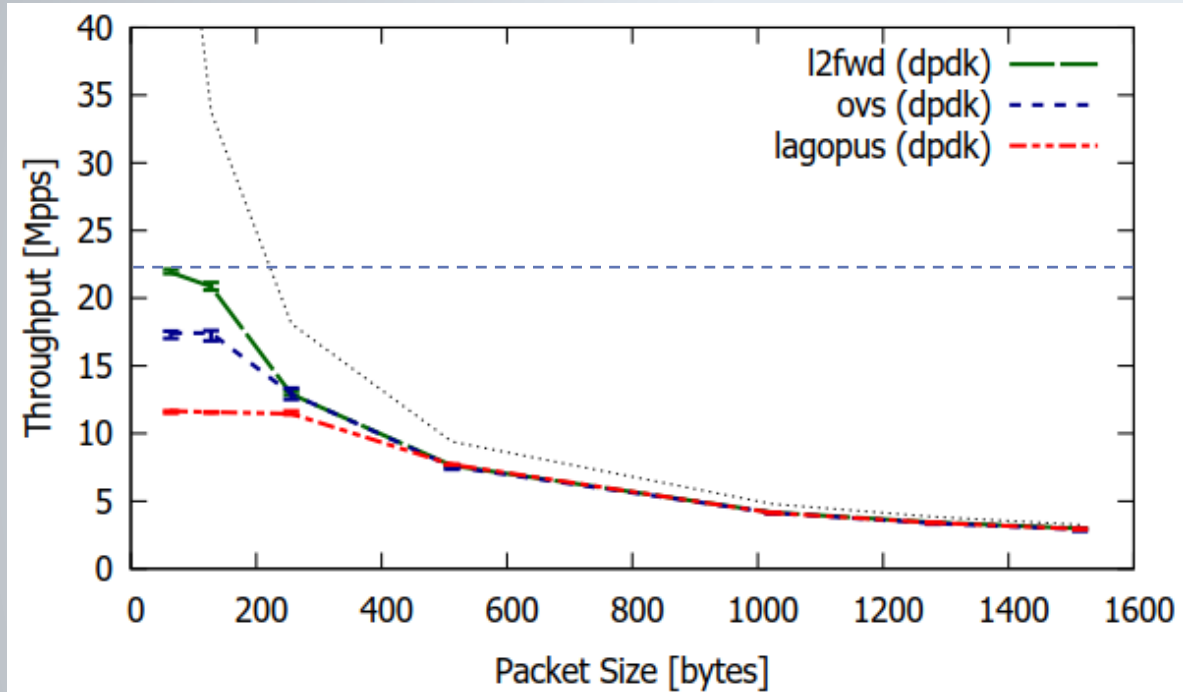
Machine 2 (2.2 GHz)



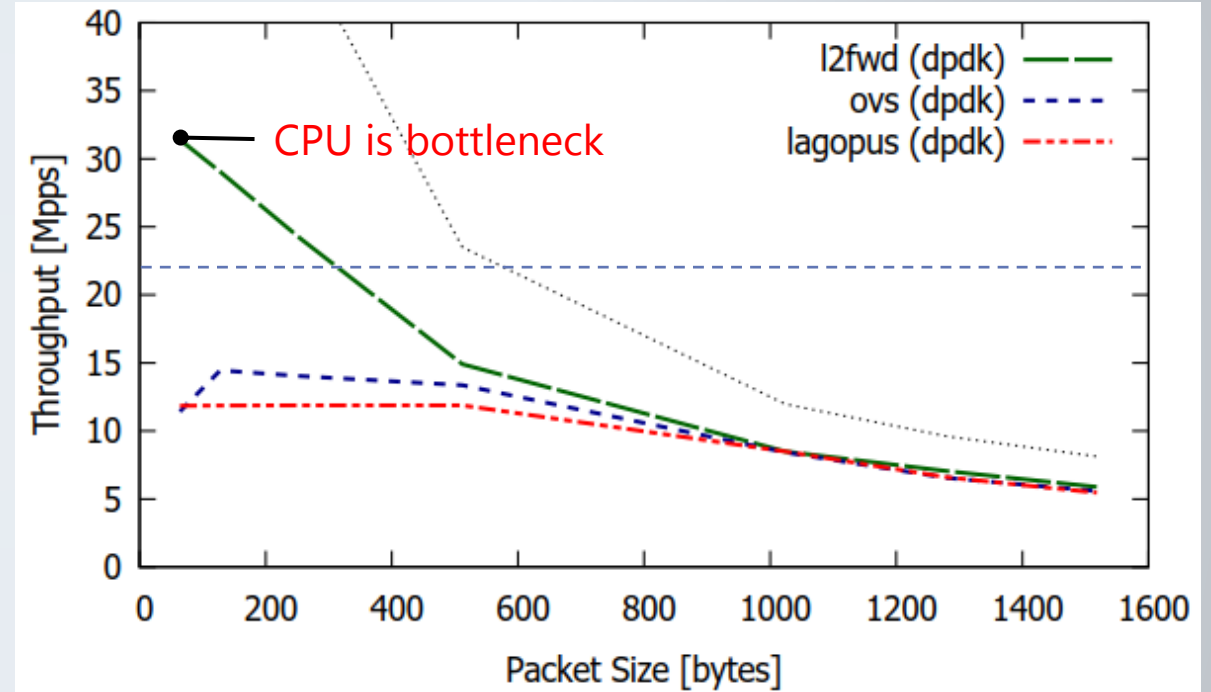
Poor throughput for short packet traffic

(Ref.) Intel XL710 vs. Mellanox ConnectX-5

Intel XL710 (40GbE)



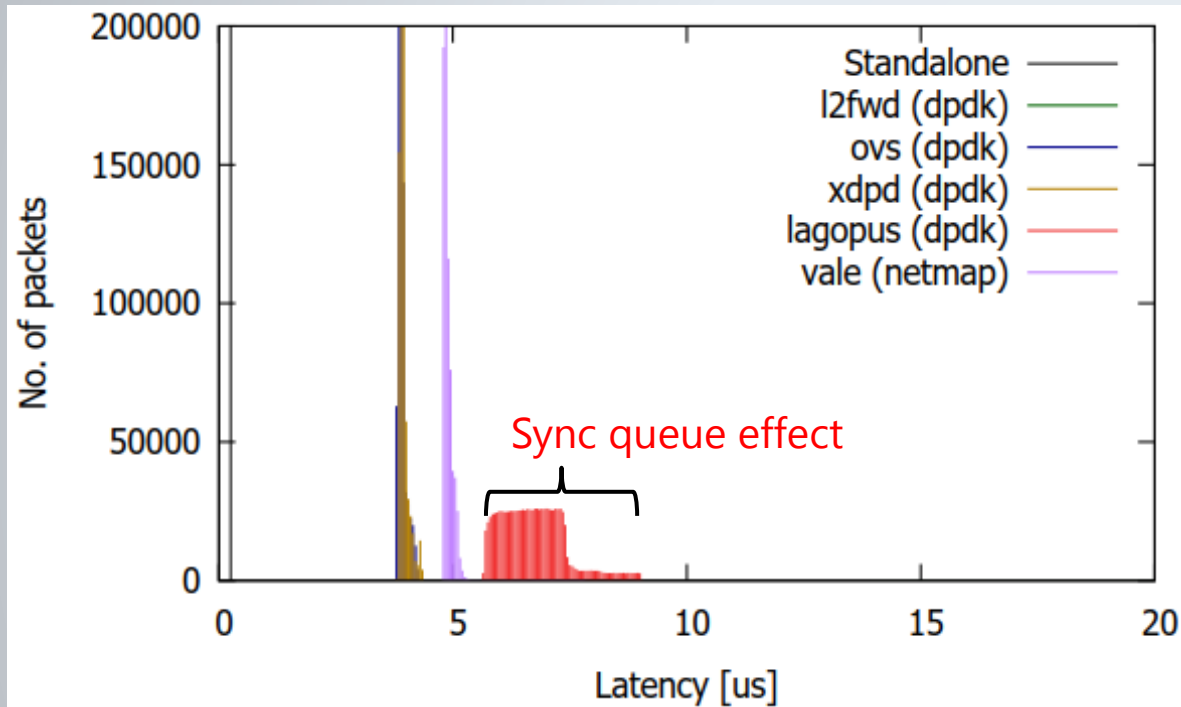
Mellanox ConnectX-5 (100GbE)



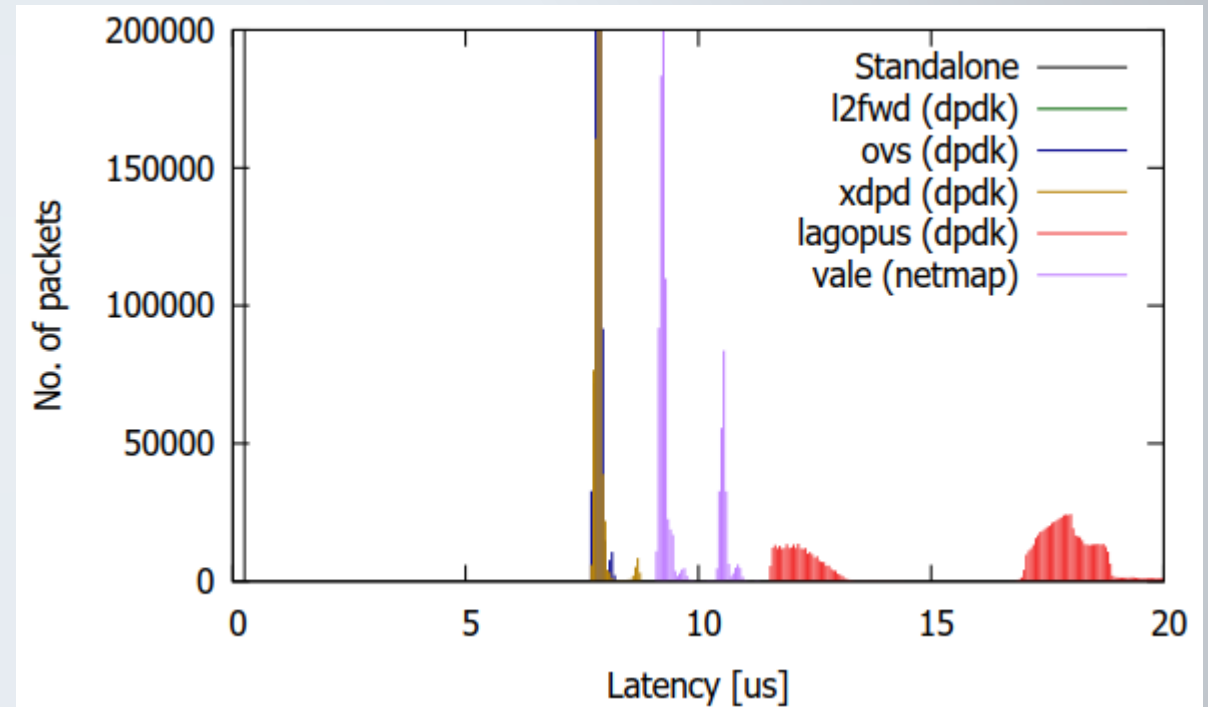
Single core can support a mere 30 Mpps

Phy-to-Phy Latency/Jitter (Baremetal)

Machine 1 (4.0 GHz)



Machine 2 (2.2 GHz)



10x latency/jitter to hardware switches

Evaluation Summary

High-clock speed CPUs

Far from **40G** throughput

A few μ s latency per node

Lessons

Learned

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Research Directions

Research Direction 1

Scale-out Approach



Aggregate Throughput

Per-datapath Throughput

Latency/Jitter



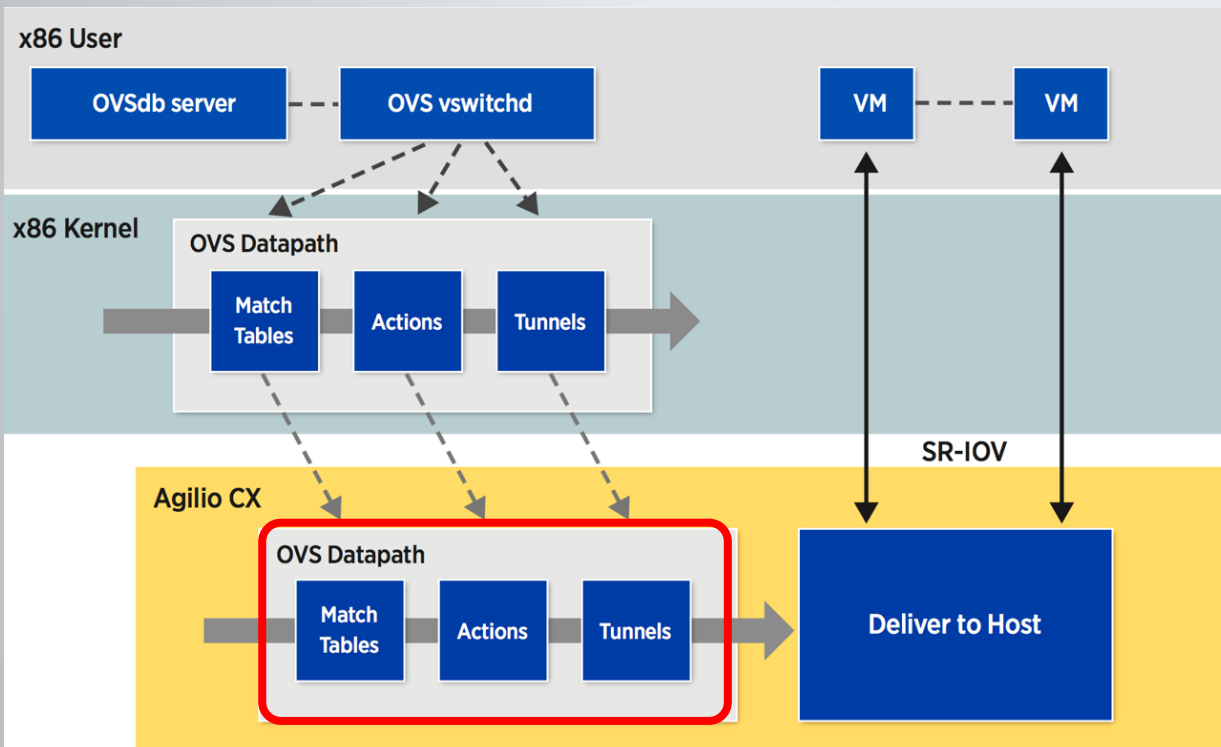
Power Consumption



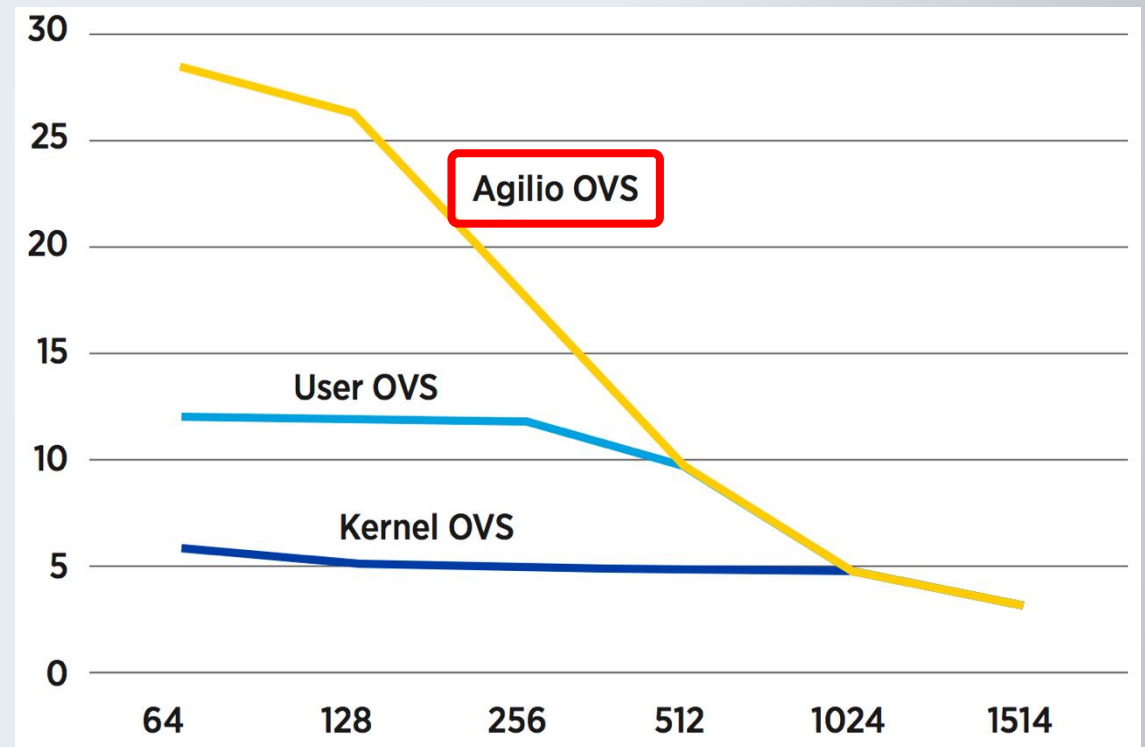
Boost Single DP Performance!

Approach 1: Hardware Offloading

NETRONOME (Smart NIC)

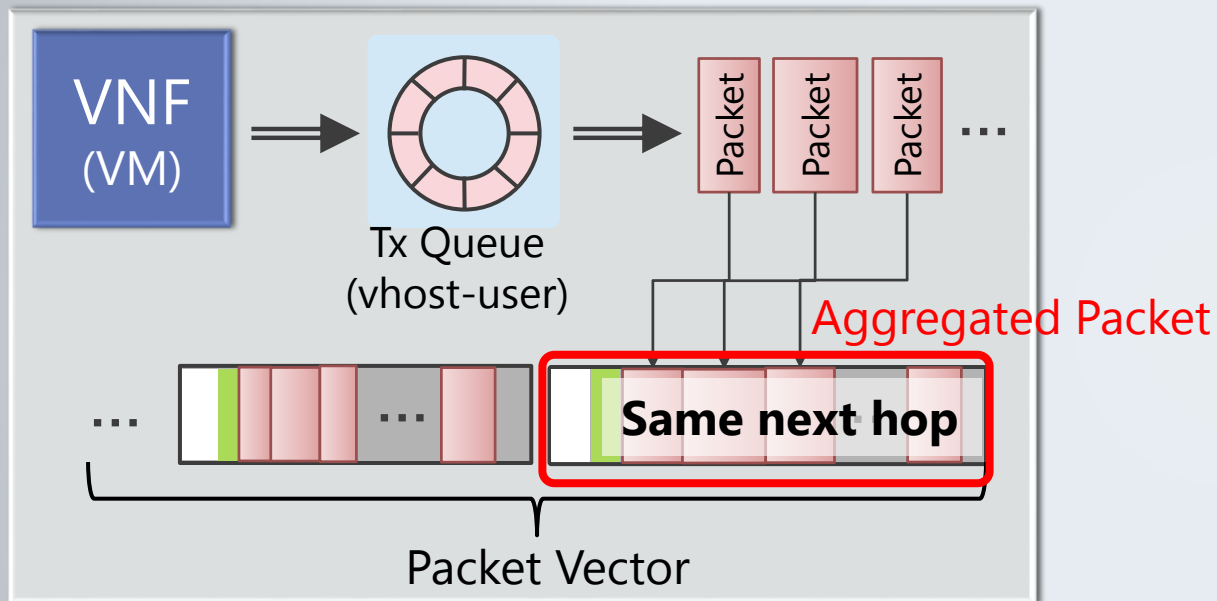


PHY-to-VM Throughput (40G)



Approach 2: Packet Aggregation

PA-Flow[†]



Traffic amount increases ...

➡ Aggregation rate increases!



Datapath Throughput

70% up!

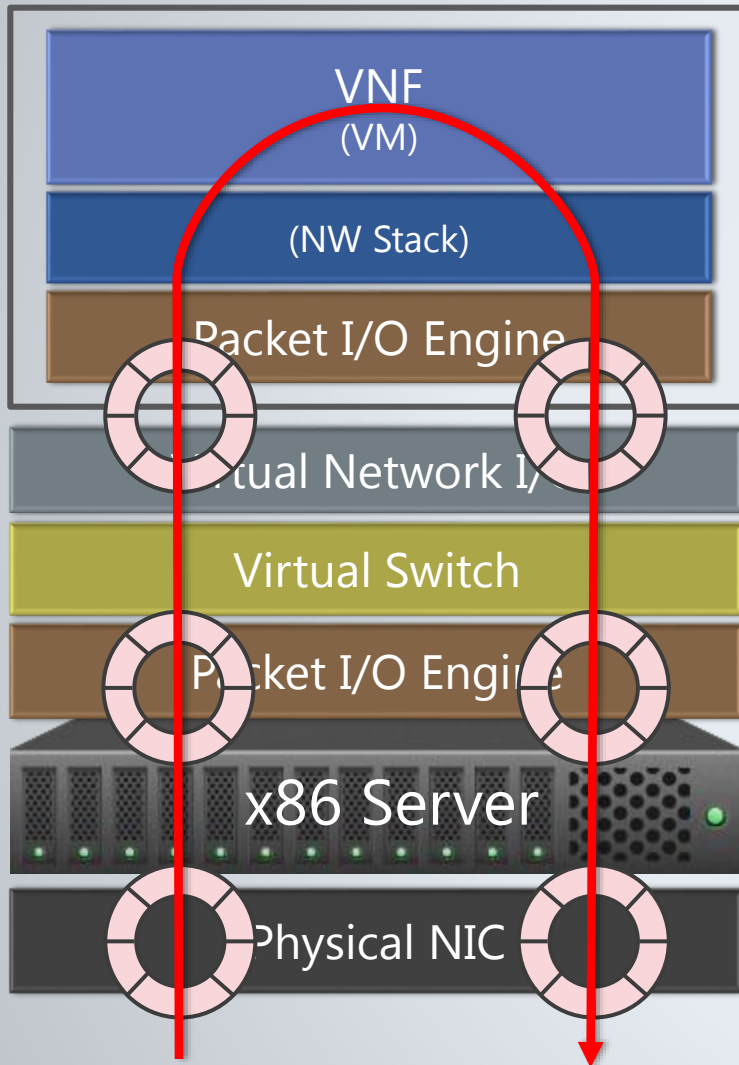


Datapath Latency

0.2μs decreases!

[†] Y. Taguchi et al., "Efficient NFV using Gradual Packet Aggregation Approach Focusing on Network I/O Processing between VMs and a Host", IEICE Tech. Rep., ICM2017-10, pp. 33-38, July 2017.

Research Direction 2

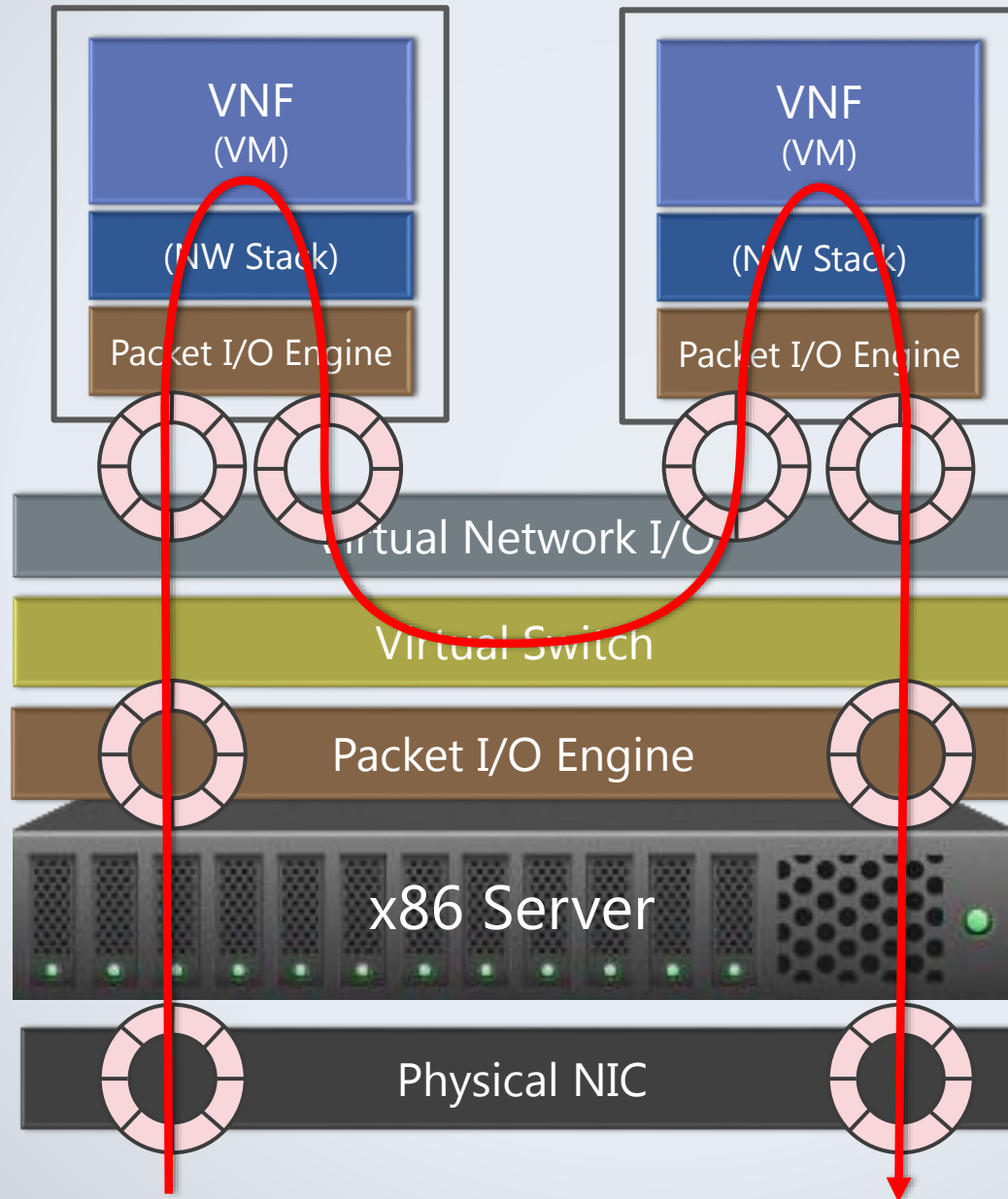


What about Service Chaining?



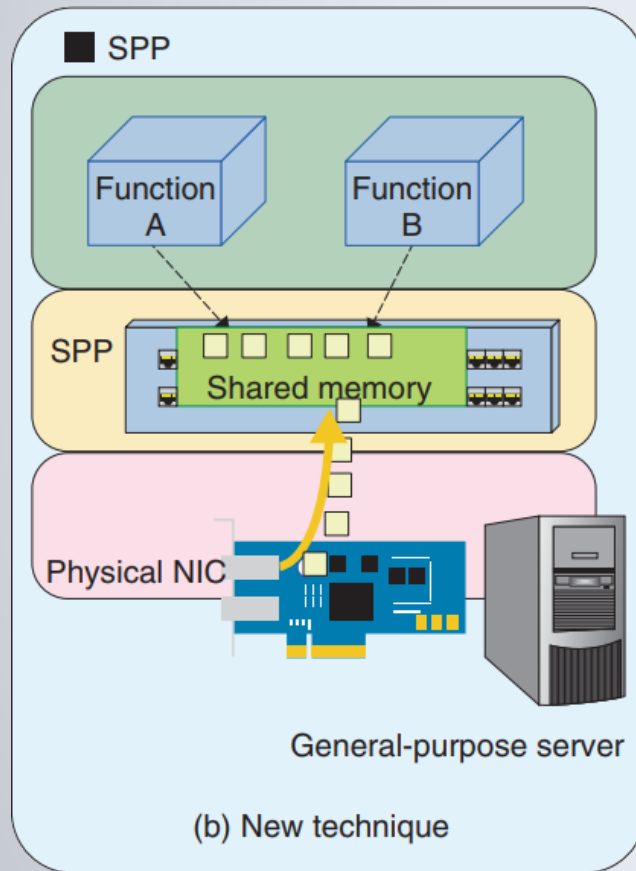
Reduce No. Enqueue Times!

Approach: Local Service Chaining

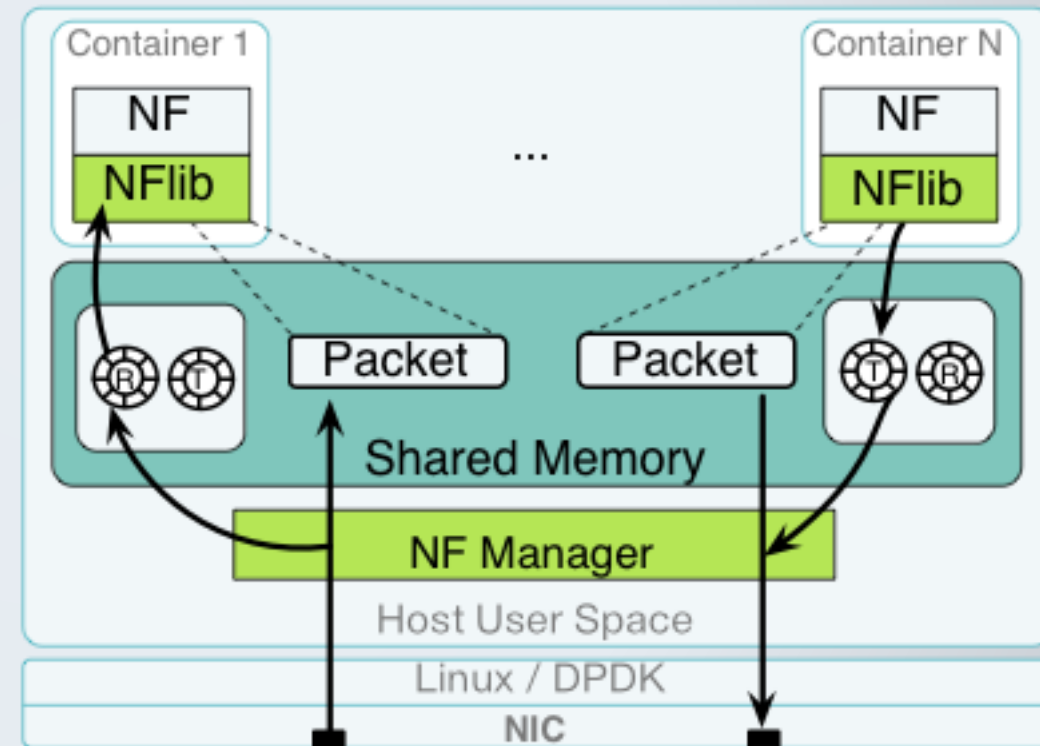


Fast Inter-VNF Communication

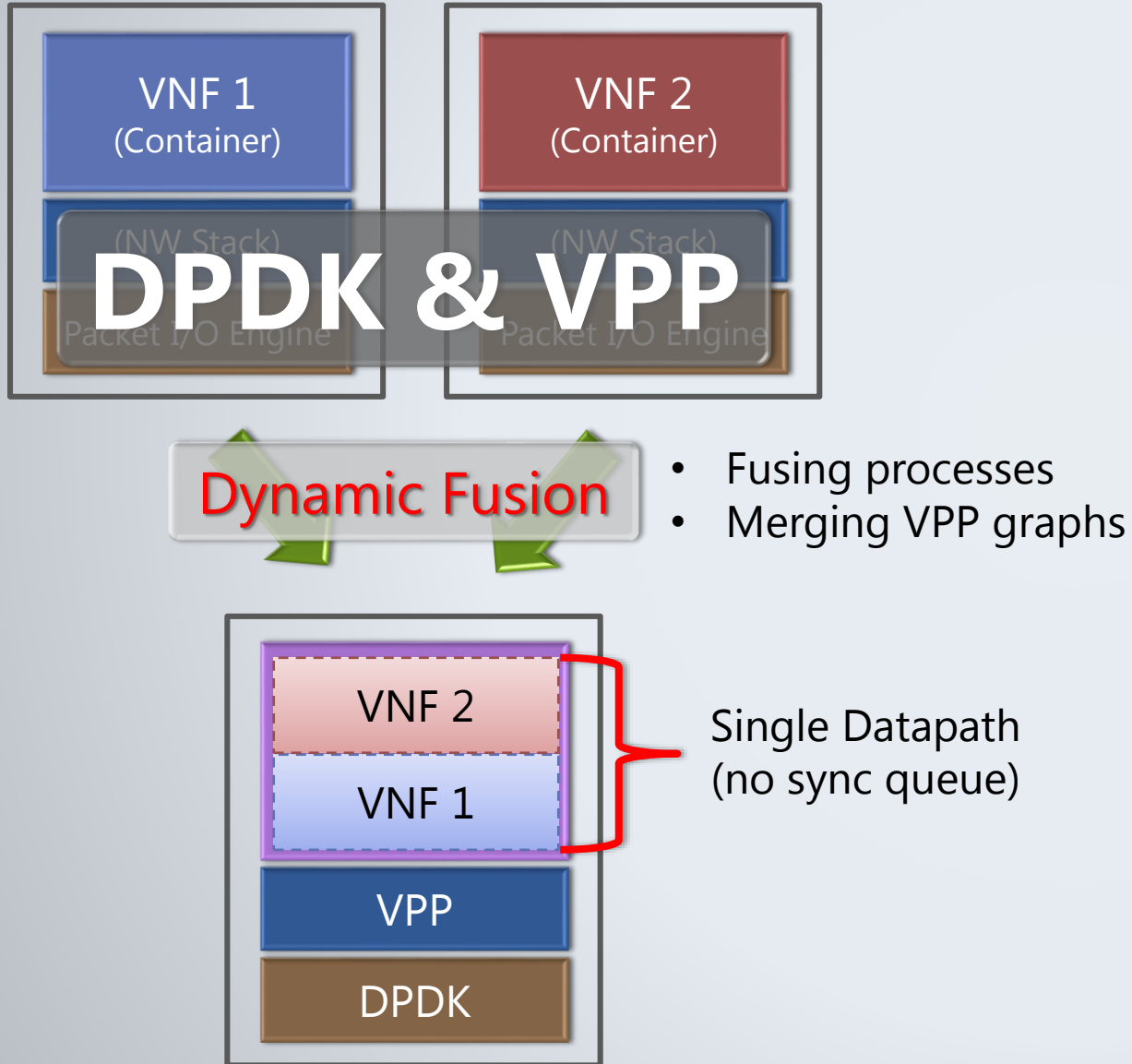
Soft Patch Panel (SPP)



openNetVM



Dynamic VNF Fusion (ultimate)



Advantages



Single DP Performance



Modularity

Challenges



Process Fusion Tech.

Summary

(Hardware Offloading)

Packet Aggregation

Boost Single DP Performance!

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Local Service Chaining

Dynamic VNF Fusion

Reduce No. Enqueue Times!